DETAILED ACTION

1. Acknowledgement is made of the amendment received on February 28, 2008. Claims 1-21 are pending in the application and have been considered below.

Allowable Subject Matter

2. Claims 1-21 are allowed.

3. The following is an examiner's statement of reasons for allowance: The present invention comprises a phase frequency detector for adjusting the target clock signal and the input/wobble signal to the same phase in an optical disc system, where the phase frequency detector comprises plurality of logic gates and flip flops. The phase of target clock signal and wobble/input signal is adjusted using the two protection signals P1 and P2 i.e. when phase modulated part of wobble signal arrives the protection signal(s) make phase frequency detector not to adjust the phase of target clock and input signal to avoid making the output unstable. The prior art Fushimi et al. (US 6,088,307) discloses a system for adjusting wobble signal a phase adjusting circuit as shown in figure 7A, but fails to disclose using a protection signal and using the components as disclosed in the present invention. Pauls (US 6,285,219) discloses a phase frequency detector with similar arrangement but fails to control the output of flip flops based on the protection signals. Brunn et al. (US 2004/0141577) discloses a phase detector using input data as input signal for flip flops with using any protection signal. The distinct

features have been added to the independent claims 1, 11 and 17. Therefore, rendering them allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Homol et al. (US 7,003,065) discloses a system and method for phase lock loop cycle slip detection with phase freq3uncy detector adjust the phase based on delay value generated from the output of logic circuits.

b. Cao (US 7,190,906) discloses a linear full rate phase detector in a clock data recovery circuit.

c. Lee (US 2004/0178834) discloses a phase locked loop circuit that update the phase of the clock signal using combination of logic values.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIRDEPAL SINGH whose telephone number is (571) 270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off) 8:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. S./
Examiner, Art Unit 2611
June 6, 2008
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611